



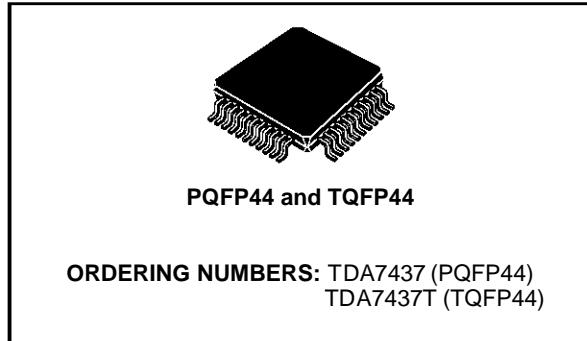
DIGITALLY CONTROLLED AUDIO PROCESSOR

- INPUT MULTIPLEXER
 - FOUR STEREO, ONE MONO INPUT, AND ONE DIFFERENTIAL INPUT
 - SELECTABLE INPUT GAIN FOR OPTIMAL ADAPTATION TO DIFFERENT SOURCES
- FULLY PROGRAMMABLE LOUDNESS FUNCTION
- VOLUME CONTROL IN 1dB STEPS INCLUDING GAIN UP TO 16dB
- ZERO CROSSING MUTE, SOFT MUTE AND DIRECT MUTE
- BASS AND TREBLE CONTROL
- FOUR SPEAKER ATTENUATORS
 - FOUR INDEPENDENT SPEAKERS CONTROL IN 1dB STEPS FOR BALANCE AND FADER FACILITIES
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL I² CBUS

DESCRIPTION

The audioprocessor TDA7437 is an upgrade of the TDA731X audioprocessor family.

Due to a highly linear signal processing, using



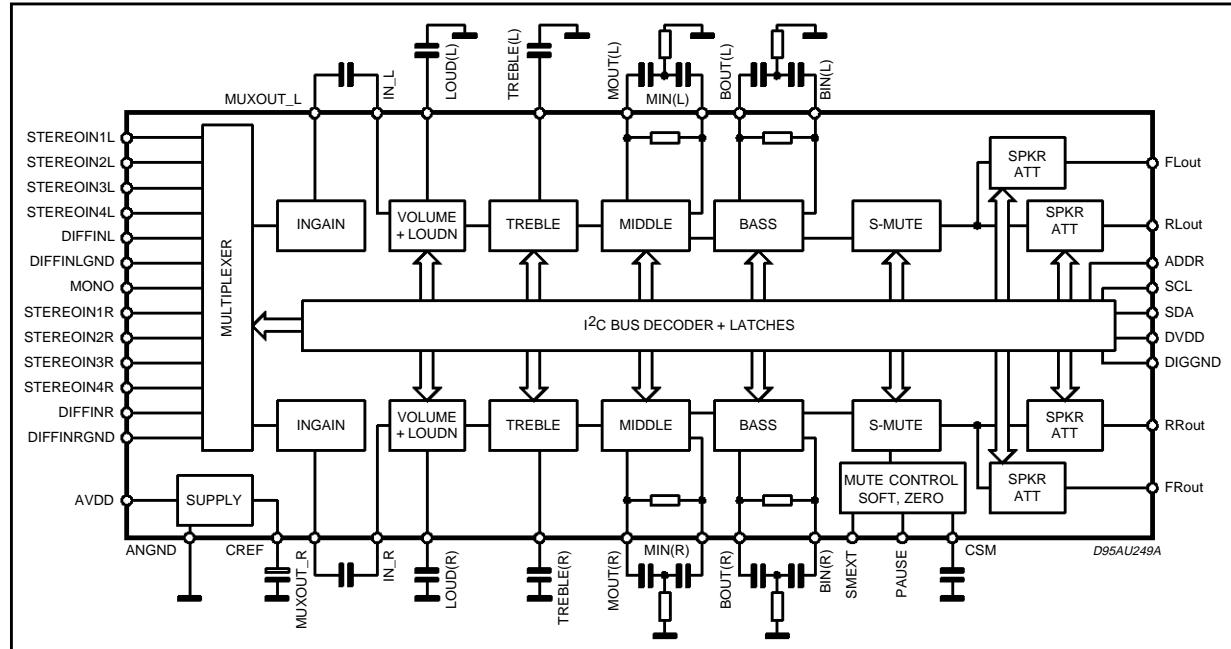
CMOS-switching techniques instead of standard bipolar multipliers, very low distortion and very low noise are obtained. Several new features like softmute, and zero-crossing mute are implemented.

The soft Mute function can be activated in two ways:

- 1 Via serial bus (Mute byte, bit D0)
- 2 Directly on pin 28 through an I/O line of the microcontroller

Very low DC stepping is obtained by use of a BICMOS technology.

BLOCK DIAGRAM

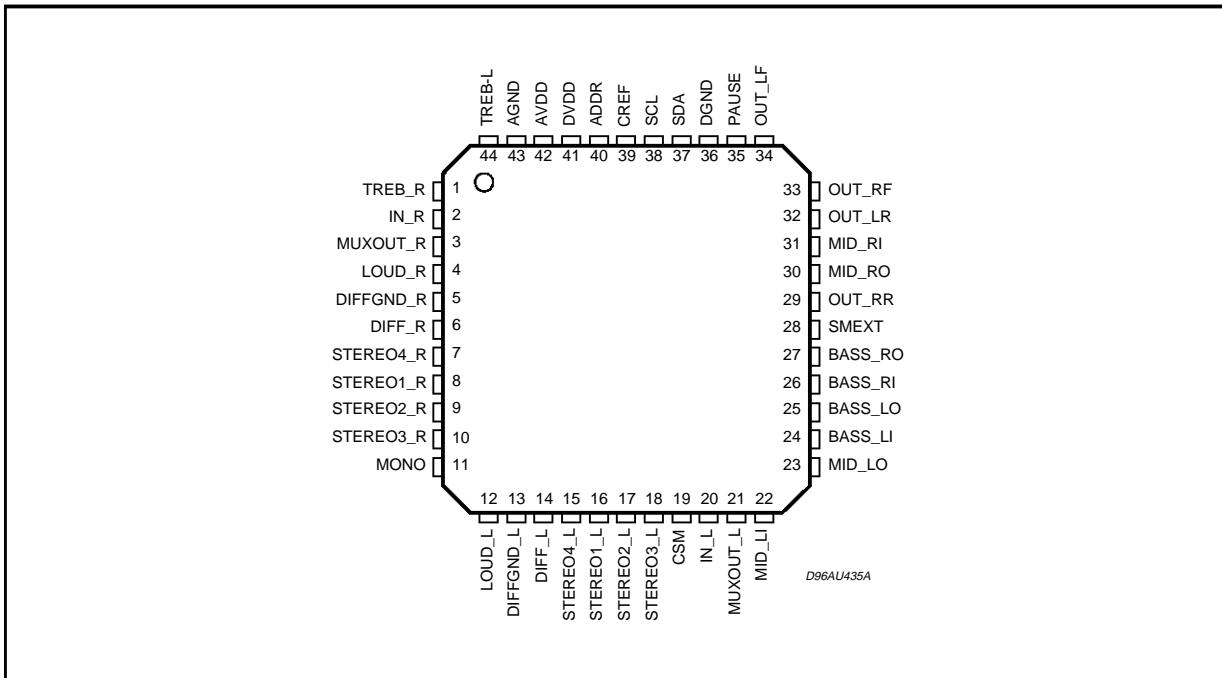


TDA7437

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	10.5	V
T_{amb}	Operating Ambient Temperature	-40 to 85	°C
T_{stg}	Storage Temperature Range	-55 to 150	°C

PIN CONNECTION



THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j-amb}$	Thermal Resistance Junction-pins	Max.	150

QUICK REFERENCE DATA

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	6	9	10.2	V
V_{CL}	Max. input signal handling	2.1	2.6		Vrms
THD	Total Harmonic Distortion V = 1Vrms f = 1KHz		0.01	0.8	%
S/N	Signal to Noise Ratio		111		dB
S_c	Channel Separation f = 1KHz		95		dB
	Input Gain 1dB step	0		15	dB
	Volume Control 1dB step	-63		16	dB
	Treble Control 2dB step	-14		+14	dB
	Bass Control 2dB step	-14		+14	dB
	Middle Control 2dB step	-14		+14	dB
	Fader and Balance Control 1dB step	-79		0	dB
	Loudness Control 1dB step	0		20	dB
	Mute Attenuation		100		dB

ELECTRICAL CHARACTERISTICS ($V_S = 9V$; $R_L = 10K\Omega$; $R_g = 50\Omega$; $T_{amb} = 25^\circ C$; all gains = 0dB; $f = 1KHz$. Refer to the test circuit, unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
--------	-----------	----------------	------	------	------	------

INPUT SELECTOR (MONO AND STEREO INPUTS)

R_I	Input Resistance	pin 7 to 11 and 15 to 18	70	100	130	$K\Omega$
V_{CL}	Clipping Level	$d \leq 0.3\%$	2.1	2.6		V_{RMS}
S_I	Input Separation		80	95		dB
R_L	Output Load Resistance		2			$K\Omega$
G_{IMIN}	Minimum Input Gain		-0.75	0	+0.75	dB
G_{IMAX}	Maximum Input Gain		14	15	16	dB
G_{step}	Step Resolution		0.5	1.0	1.5	dB
E_a	Set Error		-1.0	0	1.0	dB
V_{DC}	DC Steps	Adiacent Gain Steps		0.5	10	mV
		G_{IMIN} to G_{IMAX}		3		

DIFFERENTIAL INPUT (Pin 5, 6, 13, 14)

R_I	Input Resistance	Input selector BIT D4 = 0 (0dB)	10	15	20	$K\Omega$
		Input selector BIT D4 = 1(-6dB)	14	20	26	$K\Omega$
CMRR	Common Mode Rejection Ratio	$V_{CM} = 1V_{RMS}$; $f = 1KHz$	45	70		dB
d	Distortion	$V_I = 1V_{RMS}$		0.01	0.08	%
e_{IN}	Input Noise	20Hz to 20KHz; Flat; D6 = 0		5		μV
G_{DIFF}	Differential Gain	D4 = 0	-1	0	1	dB
		D4 = 1	-7	-6	-5	dB

VOLUME CONTROL

R_I	Input Resistance	Pin 2 and 20	31	44	57	$K\Omega$
G_{MAX}	Maximum Gain		15	16	17	dB
A_{MAX}	Maximum Attenuation		61	63.75	66.5	dB
A_{STEPC}	Step Resolution Coarse Atten.		0.5	1.0	1.5	dB
E_A	Attenuation Set Error	$G = 16$ to -20dB	-1.0	0	1.0	dB
		$G = -20$ to -63dB	-2.75		2.75	dB
E_t	Tracking Error				2	dB
V_{DC}	DC Steps	Adjacent Gain Steps	-5		+5	mV
		Adjacent Attenuation Steps	-3		+3	mV
		From 0dB to A_{MAX}		0.5	5	mV

LOUDNESS CONTROL (Pin 4, 12)

R_I	Internal Resistor	Loud = On	35	50	65	$K\Omega$
A_{MAX}	Maximum Attenuation		19	20	21	dB
A_{step}	Step Resolution		0.5	1	1.5	dB

TDA7437

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
--------	-----------	----------------	------	------	------	------

ZERO CROSSING MUTE

V_{TH}	Zero Crossing Threshold (note 1)	$WIN = 11$		30		mV
		$WIN = 10$		60		mV
		$WIN = 01$		110		mV
		$WIN = 00$		220		mV
A_{MUTE}	Mute Attenuation		80	100		dB
V_{DC}	DC Step	0dB to Mute		0.1	3	mV

SOFT MUTE

A_{MUTE}	Mute Attenuation		50	65		dB
T_{DON}	ON Delay Time	$C_{CSM} = 22nF; 0 \text{ to } -20\text{dB}; I = I_{MAX}$	0.8	1.5	2.0	ms
		$C_{CSM} = 22nF; 0 \text{ to } -20\text{dB}; I = I_{MIN}$	25	45	60	ms
T_{DOFF}	OFF Current	$V_{CSM} = 0V; I = I_{MAX}$	20	40	60	μA
		$V_{CSM} = 0V; I = I_{MIN}$		2		μA
R_{INT}	Pullup Resistor (pin 28)	(note 2)		100		$K\Omega$
V_{SMH}	(pin 28) Level High		3.5			V
V_{SML}	(pin 28) Level Low	Soft Mute Active			1	V

BASS CONTROL

C_{range}	Control Range		± 11.5	± 14	± 16	dB
A_{step}	Step Resolution		1	2	3	dB
R_g	Internal Feedback Resistance		31	44	57	$K\Omega$

MIDDLE CONTROL

C_{range}	Control Range		± 11.5	± 14	± 16	dB
A_{step}	Step Resolution		1	2	3	dB
R_g	Internal Feedback Resistance		17.5	25	32.5	$K\Omega$

TREBLE CONTROL

C_{range}	Control Range		± 13	± 14	± 15	dB
A_{step}	Step Resolution		1	2	3	dB

SPEAKER ATTENUATORS

C_{range}	Control Range			79		dB
A_{step}	Step Resolution	$A_V = 0 \text{ to } -40\text{dB}$	0.5	1	1.5	dB
A_{MUTE}	Output Mute Attenuation	Data Word = 1111XXXX	80	100		dB
E_A	Attenuation Set Error	$A_V = 0 \text{ to } -40\text{dB}$			1.5	dB
V_{DC}	DC Steps	Adjacent Attenuation Steps		0.1	3	mV

AUDIO OUTPUT

V_{clip}	Clipping Level	$d = 0.3\%$	2.1	2.6		Vrms
R_L	Output Load Resistance		2			$K\Omega$
R_O	Output Impedance		50	90	140	Ω
V_{DC}	DC Voltage Level		3.5	3.8	4.1	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
GENERAL						
V_{CC}	Supply Voltage		6	9	10.2	V
I_{CC}	Supply Current		7	10	13	mA
PSRR	Power Supply Rejection Ratio	$f = 1\text{KHz}$	70	90		dB
e_{NO}	Output Noise	Output Muted ($B = 20$ to 20kHz flat)		4		μV
		All Gains 0dB ($B = 200$ to 20kHz flat)		6	15	μV
E_t	Total Tracking Error	$A_V = 0$ to -20dB		0	1	dB
		$A_V = -20$ to -60dB		0	2	dB
S/N	Signal to Noise Ratio	All Gains = 0dB; $V_O = 2.1V_{rms}$		111		dB
S_C	Channel Separation L - R		80	95		dB
d	Distortion	$V_{IN} = 1\text{V}$ all gain = 0dB		0.01	0.08	%

BUS INPUTS

V_{IL}	Input Low Voltage				1	V
V_{IN}	Input High Voltage		3			V
I_{IN}	Input Current	$V_{IN} = 0.4\text{V}$	-5		5	μA
V_O	Output Voltage SDA Acknowledge	$I_O = 1.6\text{mA}$		0.1	0.4	V

Note 1: WIN represents the MUTE programming bit pair D₆, D₅ for the zero crossing window threshold

Note 2: Internal pullup resistor to Vs/2; "LOW" = softmute active

I²C BUS INTERFACE

Data transmission from microprocessor to the TDA7437 and viceversa takes place thru the 2 wires I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be externally connected).

Data Validity

As shown in fig. 3, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Start and Stop Conditions

As shown in fig.4 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH. A STOP conditions must be sent before each START condition.

Byte Format

Every byte transferred to the SDA line must con-

tain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

Acknowledge

The master (μ P) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 5). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

Transmission without Acknowledge

Avoiding to detect the acknowledge of the audioprocessor, the μ P can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking and decreases the noise immunity.

Figure 3: Data Validity on the I²CBUS

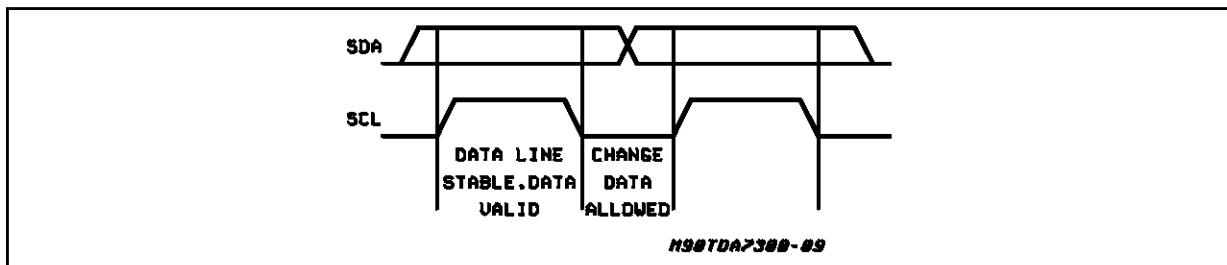


Figure 4: Timing Diagram of I²CBUS

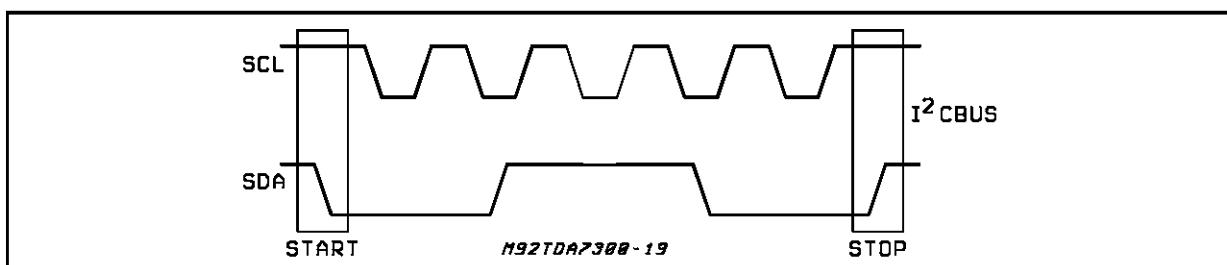
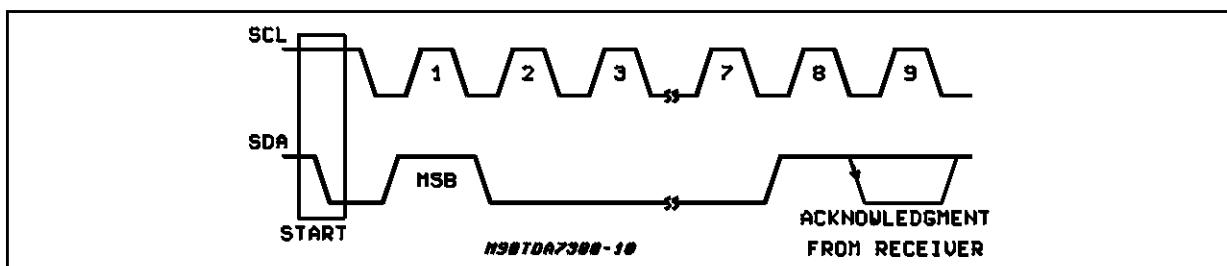


Figure 5: Acknowledge on the I²CBUS



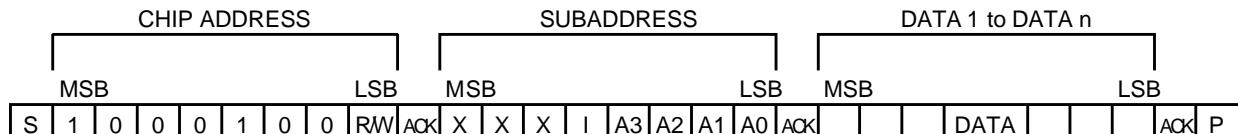
SOFTWARE SPECIFICATION**Interface Protocol**

The interface protocol comprises:

- A start condition (s)
- A chip address byte,(the LSB bit determines

read/write transmission)

- A subaddress byte.
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)



ACK = Acknowledge

S = Start

P = Stop

I = Auto Increment

X = Not used

MAX CLOCK SPEED 500kbits/s

AUTO INCREMENT

If bit I in the subaddress byte is set to "1", the autoincrement of the subaddress is enabled

SUBADDRESS (receive mode)

MSB								LSB	FUNCTION
X	X	X	I	A3	A2	A1	A0		
				0	0	0	0		Input Selector
				0	0	0	1		Loudness
				0	0	1	0		Volume
				0	0	1	1		Bass, Treble
				0	1	0	0		Speaker Attenuator LF
				0	1	0	1		Speaker Attenuator LR
				0	1	1	0		Speaker Attenuator RF
				0	1	1	1		Speaker Attenuator RR
				1	0	0	0		Input Gain Middle
				1	0	0	1		Mute

TRANSMITTED DATA

Send Mode

MSB							LSB
X	X	X	X	X	SM	ZM	X

ZM = Zero crossing muted (HIGH active)

SM = Soft mute activated (HIGH active)

X = Not used

The transmitted data is automatically updated after each ACK.

Transmission can be repeated without new chipaddress.

TDA7437

DATA BYTE SPECIFICATION

Input Selector

MSB								LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0		
				1	0	0	0		DIFFERENTIAL
				1	0	0	1		STEREO 1
				1	0	1	0		STEREO 2
				1	0	1	1		STEREO 3
				1	1	0	0		STEREO 4
				1	1	0	1		MONO
X	X	X	X	0	X	X	X		DC CONNECT
		0	0						HALF-DIFF 0dB
		0	1						HALF-DIFF -6dB
		1	0						FULL-DIFF 0dB
		1	1						FULL-DIFF -6dB

Loudness

MSB								LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0		LOUDNESS STEP
		0	0	0	0	0	0		0dB
		0	0	0	0	0	1		1dB
		0	0	0	0	1	0		2dB
		0	0	0	0	1	1		3dB
		0	0	0	1	0	0		4dB
		0	0	0	1	0	1		5dB
		0	0	0	1	1	0		6dB
		0	0	0	1	1	1		7dB
		0	0	1	0	0	0		8dB
		0	0	1	0	0	1		9dB
		0	0	1	0	1	0		10dB
		0	0	1	0	1	1		11dB
		0	0	1	1	0	0		12dB
		0	0	1	1	0	1		13dB
		0	0	1	1	1	0		14dB
		0	0	1	1	1	1		15dB
		0	1	0	0	0	0		16dB
		0	1	0	0	0	1		17dB
		0	1	0	0	1	0		18dB
		0	1	0	0	1	1		19dB
		0	1	0	1	0	0		20dB
		1							LOUDNESS OFF
									FINE VOLUME
0	0								0dB
0	1								-0.25dB
1	0								-0.5dB
1	1								-0.75dB

Mute

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
				0			1	Soft Mute On
				0		0	1	Soft Mute with fast slope
				0		1	1	Soft Mute with slow slope
			0	0	1			Zero Mute
				1				Direct Mute
				1				Reset
0	0	0						Zero (160mV)
0	1	0						Zero (80mV)
1	0	0						Zero (40mV)
1	1	0						Zero (20mV)
0								Nonsymmetrical Bass
1								Symmetrical Bass

Volume

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
1					0	0	0	0dB
1					0	0	1	-1dB
1					0	1	0	-2dB
1					0	1	1	-3dB
1					1	0	0	-4dB
1					1	0	1	-5dB
1					1	1	0	-6dB
1					1	1	1	-7dB
1								
1	0	0	0	0				16dB
1	0	0	0	1				8dB
1	0	0	1	0				0dB
1	0	0	1	1				-8dB
1	0	1	0	0				-16dB
1	0	1	0	1				-24dB
1	0	1	1	0				-32dB
1	0	1	1	1				-40dB
1	1	0	0	0				-48dB
1	1	0	0	1				-56dB
0	X	X	X	X	X	X	X	MUTE

TDA7437

Speaker

MSB								LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0		
									1.25dB step
					0	0	0		0dB
					0	0	1		-1dB
					0	1	0		-2dB
					0	1	1		-3dB
					1	0	0		-4dB
					1	0	1		-5dB
					1	1	0		-6dB
					1	1	1		-7dB
0	0	0	0						0dB
0	0	0	1						-8dB
0	0	1	0						-16dB
0	0	1	1						-24dB
0	1	0	0						-32dB
0	1	0	1						-40dB
0	1	1	0						-48dB
0	1	1	1						-56dB
1	0	0	0						-64dB
1	0	0	1						-72dB
1	1	1	1	X	X	X			MUTE

Bass Treble

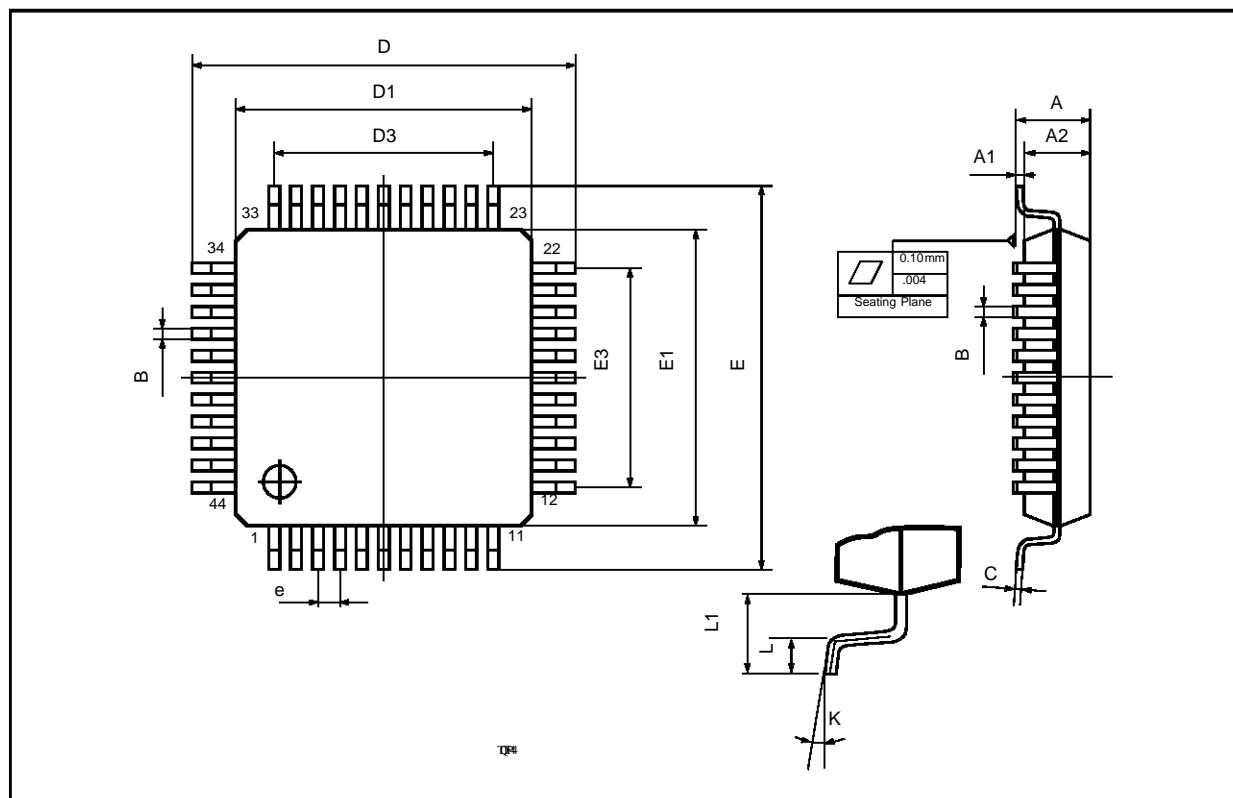
MSB	D7	D6	D5	D4	D3	D2	D1	LSB	FUNCTION
	D0								
TREBLE STEP									
					0	0	0	0	-14dB
					0	0	0	1	-12dB
					0	0	1	0	-10dB
					0	0	1	1	-8dB
					0	1	0	0	-6dB
					0	1	0	1	-4dB
					0	1	1	0	-2dB
					0	1	1	1	0dB
					1	1	1	1	0dB
					1	1	1	0	2dB
					1	1	0	1	4dB
					1	1	0	0	6dB
					1	0	1	1	8dB
					1	0	1	0	10dB
					1	0	0	1	12dB
					1	0	0	0	14dB
BASS STEPS									
0	0	0	0						-14dB
0	0	0	1						-12dB
0	0	1	0						-10dB
0	0	1	1						-8dB
0	1	0	0						-6dB
0	1	0	1						-4dB
0	1	1	0						-2dB
0	1	1	1						0dB
1	1	1	1						0dB
1	1	1	0						2dB
1	1	0	1						4dB
1	1	0	0						6dB
1	0	1	1						8dB
1	0	1	0						10dB
1	0	0	1						12dB
1	0	0	0						14dB

Input Stage Gain Middle

MSB	D7	D6	D5	D4	D3	D2	D1	LSB	FUNCTION
	D0								
							IN-GAIN STEP		
					0	0	0	0	0dB
					0	0	0	1	1dB
					0	0	1	0	2dB
					0	0	1	1	3dB
					0	1	0	0	4dB
					0	1	0	1	5dB
					0	1	1	0	6dB
					0	1	1	1	7dB
					1	0	0	0	8dB
					1	0	0	1	9dB
					1	0	1	0	10dB
					1	0	1	1	11dB
					1	1	0	0	12dB
					1	1	0	1	13dB
					1	1	1	0	14dB
					1	1	1	1	15dB
							MIDDLE STEP		
0	0	0	0						-14dB
0	0	0	1						-12dB
0	0	1	0						-10dB
0	0	1	1						-8dB
0	1	0	0						-6dB
0	1	0	1						-4dB
0	1	1	0						-2dB
0	1	1	1						0dB
1	1	1	1						0dB
1	1	1	0						2dB
1	1	0	1						4dB
1	1	0	0						6dB
1	0	1	1						8dB
1	0	1	0						10dB
1	0	0	1						126B
1	0	0	0						14dB

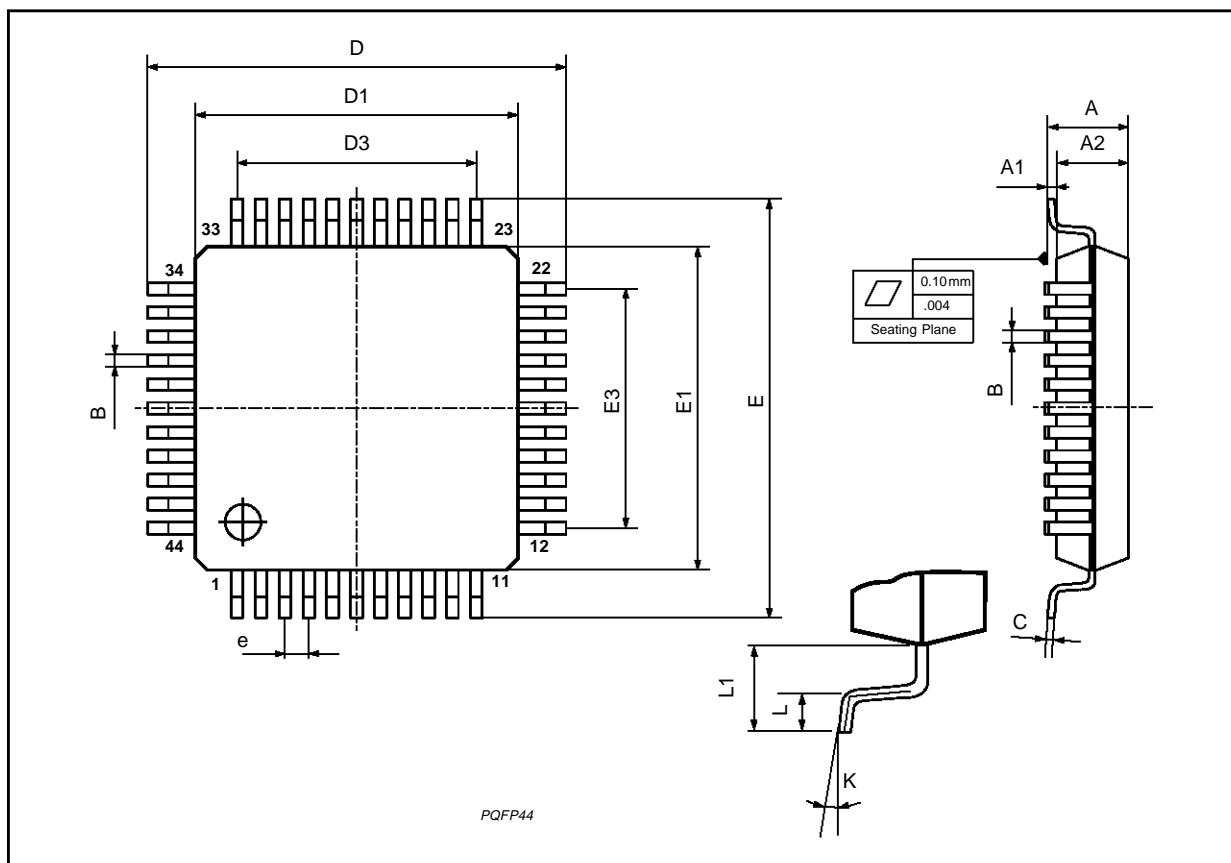
TQFP44 (10 x 10) PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.014	0.018
C	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
D3		8.00			0.315	
e		0.80			0.031	
E		12.00			0.472	
E1		10.00			0.394	
E3		8.00			0.315	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0°(min.), 3.5°(typ.), 7°(max.)					



PQFP44 (10 x10) PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.45			0.096
A1	0.25			0.010		
A2	1.95	2.00	2.10	0.077	0.079	0.083
B	0.30		0.45	0.012		0.018
c	0.13		0.23	0.005		0.009
D	12.95	13.20	13.45	0.51	0.52	0.53
D1	9.90	10.00	10.10	0.390	0.394	0.398
D3		8.00			0.315	
e		0.80			0.031	
E	12.95	13.20	13.45	0.510	0.520	0.530
E1	9.90	10.00	10.10	0.390	0.394	0.398
E3		8.00			0.315	
L	0.65	0.80	0.95	0.026	0.031	0.037
L1		1.60			0.063	
K	0°(min.), 7°(max.)					



Purchase of I²C Components of SGS-THOMSON Microelectronics, conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specifications as defined by Philips.

Information furnished is believed to be accurate and reliable. However, SGS-THOMSON Microelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of SGS-THOMSON Microelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. SGS-THOMSON Microelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of SGS-THOMSON Microelectronics.

© 1996 SGS-THOMSON Microelectronics – Printed in Italy – All Rights Reserved
SGS-THOMSON Microelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - France - Germany - Hong Kong - Italy - Japan - Korea - Malaysia - Malta - Morocco - The Netherlands - Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.